Abstracts

Generating PBR Sequences for System Testing at 500megabits/Sec. and Higher Using IC Flip-Flops.

J.A. Coekin and J.R. Wicking. "Generating PBR Sequences for System Testing at 500megabits/Sec. and Higher Using IC Flip-Flops.." 1972 G-MTT International Microwave Symposium Digest of Technical Papers 72.1 (1972 [MWSYM]): 207-210.

Generating pseudo-random bit sequences at very high bit-rates is limited by the maximum switching speed of shift registers and modulo-2 adders. A system is proposed in which registers composed of integrated circuits, operating near their maximum bit-rate may be combined in parallel to produce sequences at much higher rates.

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